WHAT IS CLAIMED IS:

1. A semiconductor memory device operable in a normal output mode and a test output mode, comprising:

a first array of memory cells;

a first array of sense amplifiers for reading data from the first array of memory cells;

a plurality of column lines coupled to the first array of sense amplifiers, each column line selecting at least two of the sense amplifiers in the first array of sense amplifiers;

a plurality of data bus lines receiving the data read by the selected sense amplifiers in the first array of sense amplifiers;

a first decision circuit receiving and comparing data read by two of the selected sense amplifiers in the first array of sense amplifiers and generating comparison result data; and

a first input-output buffer receiving data from at least one of the data bus lines in the normal output mode, receiving the comparison result data from the first decision circuit in the test output mode, and providing external output of the received data.

2. The semiconductor memory device of claim 1, further comprising a test data bus line linking the first decision circuit to the first input-output buffer.

3. The semiconductor memory device of claim 2, wherein the data bus lines include a complementary pair of data bus lines and the test data bus line is disposed between the complementary pair of data bus lines.

4. The semiconductor memory device of claim 1, further

comprising:

a redundant array of memory cells;

a plurality of redundant sense amplifiers for reading data from the redundant array of memory cells and supplying the read data to the data bus lines;

a redundancy decision circuit programmable to replace at least two of the sense amplifiers in the first array of sense amplifiers with at least two of the redundant sense amplifiers.

5. The semiconductor memory device of claim 1, further comprising:

a second array of sense amplifiers for reading data from the first array of memory cells, each column line also selecting at least two of the sense amplifiers in the second array of sense amplifiers;

a second decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the second array of sense amplifiers and generating comparison result data; and

a second input-output buffer receiving data from at least another one of the data bus lines in the normal output mode, receiving the comparison result data from the second decision circuit in the test output mode, and providing external output of the received data.

6. The semiconductor memory device of claim 5, further comprising:

a redundant array of memory cells;

a plurality of first redundant sense amplifiers for reading data from the redundant array of memory cells and supplying the read data to the data bus lines;

a first redundancy decision circuit programmable to replace at least two of the sense amplifiers in the first

array of sense amplifiers with at least two of the first redundant sense amplifiers.

a plurality of second redundant sense amplifiers for reading data from the redundant array of memory cells and supplying the read data to the data bus lines; and

a second redundancy decision circuit programmable to replace at least two of the sense amplifiers in the second array of sense amplifiers with at least two of the second redundant sense amplifiers.

7. The semiconductor memory device of claim 1, further comprising:

a second array of memory cells;

a second array of sense amplifiers for reading data from the second array of memory cells, each column line also selecting at least two of the sense amplifiers in the second array of sense amplifiers, the first and second arrays of sense amplifiers both providing data to the same plurality of data bus lines;

a second decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the second array of sense amplifiers and generating comparison result data; and

a second input-output buffer receiving data from at least another one of the data bus lines in the normal output mode, receiving the comparison result data from the second decision circuit in the test output mode, and providing external output of the received data.

8. The semiconductor memory device of claim 1, further comprising:

second, third, and fourth arrays of memory cells;

a second array of sense amplifiers selectable at least two at a time by the column signal lines, for reading data

from the first memory cell array and the second memory cell array;

a third array of sense amplifiers selectable at least two at a time by the column signal lines, for reading data from the second memory cell array and the third memory cell array;

a fourth array of sense amplifiers selectable at least two at a time by the column signal lines, for reading data from the third memory cell array and the fourth memory cell array;

a fifth array of sense amplifiers selectable at least two at a time by the column signal lines, for reading data from the fourth memory cell array;

a second decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the second array of sense amplifiers and generating comparison result data;

a third decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the third array of sense amplifiers and generating comparison result data;

a fourth decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the fourth array of sense amplifiers and generating comparison result data;

a fifth decision circuit for receiving and comparing data read by two of the selected sense amplifiers in the fifth array of sense amplifiers and generating comparison result data;

a second input-output buffer receiving data from at least another one of the data bus lines in the normal output mode, receiving the comparison result data from the second decision circuit in the test output mode, and providing external output of the received data;

a third input-output buffer receiving data from at least yet another one of the data bus lines in the normal output mode, receiving the comparison result data from the third decision circuit in the test output mode, and providing external output of the received data; and

a fourth input-output buffer receiving data from at least still another one of the data bus lines in the normal output mode, receiving the comparison result data from the fourth decision circuit in the test output mode, and providing external output of the received data;

wherein the first input-output buffer also receives the comparison result data from the fifth decision circuit; and

in the test output mode, data are read simultaneously either from the first and third arrays of memory cells, or from the second and fourth arrays of memory cells.

9. A semiconductor memory device operable in a normal output mode and a first test output mode, comprising:

a plurality of column signal lines;

a plurality of arrays of sense amplifiers, the sense amplifiers in each array being selectable at least two at a time by the column signal lines;

a plurality of memory cell arrays interspersed among the sense amplifier arrays so that data stored in each memory cell array are read by sense amplifiers in two adjacent arrays of sense amplifiers;

a plurality of data bus lines for receiving data read from the memory cell arrays by the sense amplifiers in the sense amplifier arrays;

a plurality of primary decision circuits connected to respective arrays of sense amplifiers, each primary decision circuit comparing data read by two of the selected sense amplifiers in the connected one of the arrays of sense amplifiers and generating first comparison result data;

a plurality of secondary decision circuits for comparing the first comparison result data generated by adjacent pairs of the primary decision circuits and generating second comparison result data; and

a plurality of input-output buffers receiving data from the data bus lines in the normal output mode, receiving the second comparison result data from the secondary decision circuits in the first test output mode, and providing external output of the received data.

10. The semiconductor memory device of claim 9, further comprising a plurality of test data bus lines linking the secondary decision circuits to the input-output buffers.

11. The semiconductor memory device of claim 10, wherein each of the test data bus lines is disposed between a pair of the data bus lines, different test data bus lines being disposed between different pairs of the test data bus lines.

12. The semiconductor memory device of claim 9, further comprising:

a plurality of redundant arrays of memory cells;

a plurality of redundant sense amplifiers for reading data from the redundant arrays of memory cells and supplying the read data to the data bus lines;

a plurality of redundancy decision circuits, each redundancy decision circuit being programmable to replace at least two of the sense amplifiers in each of two adjacent arrays of sense amplifiers with at least two of the redundant sense amplifiers.

13. The semiconductor memory device of claim 9, wherein there are N input-output buffers and at least 2N memory cell arrays, N being a positive integer, the memory cell arrays

being tested N at a time in the first test output mode.

14. The semiconductor memory device of claim 9, also operable in a second test output mode in which the input-output buffers receive first comparison result data from the primary decision circuits, and provide external output of the received data.

15. The semiconductor memory device of claim 14, wherein there are N input-output buffers and at least 2N memory cell arrays, N being an even positive integer, the memory cell arrays being tested N at a time in the first test output mode and N/2 at a time in the second test output mode.

16. The semiconductor memory device of claim 14, further comprising:

a plurality of redundant arrays of memory cells;

a plurality of redundant sense amplifiers for reading data from the redundant arrays of memory cells and supplying the read data to the data bus lines;

a plurality of redundancy decision circuits, each redundancy decision circuit being programmable to replace at least two of the sense amplifiers in one of the arrays of sense amplifiers with at least two of the redundant sense amplifiers.

17. The semiconductor memory device of claim 16, wherein the second test output mode is used to obtain information for programming the redundancy decision circuits, and the first test output mode is used for pass-fail inspection of the semiconductor memory device.

18. The semiconductor memory device of claim 9, wherein the input-output buffers include a first group of input-output

buffers and a second group of input-output buffers, use of the second group of input-output buffers for external output being optional, the first group of input-output buffers providing external output of data received by the second group of input-output buffers when the second group of input-output buffers are not used for external output, the semiconductor memory device further comprising:

a plurality of tertiary decision circuits for comparing the second comparison result data generated by pairs of the secondary decision circuits, generating third comparison result data, and supplying the third comparison result data to the first group of input-output buffers when the second group of input-output buffers are not used for external output.

19. The semiconductor memory device of claim 18, further comprising a block select signal line for selecting all of the memory cell arrays, thereby enabling data input through the first group of input-output buffers to be written into all of the memory cell arrays simultaneously.